REMARKS

The following remarks are made in response to the Non-Final Office Action mailed April 19, 2007. Claims 22-43 were rejected. With this Response, claims 22-25 and 27-43 have been amended. Claims 22-25 and 27-43 remain pending in the application and are presented for reconsideration and allowance.

In the Drawings

The Examiner objected to the drawings under 37 C.F.R. 1.83(a). The drawings must show every feature of the invention specified in the claims. In particular, the Examiner has stated that the "sub region of the via hole that does not have the nanostructure" must be shown or the feature(s) cancelled from the claims(s)."

Claim 38, the only claim that recited the "sub region of the via hole that does not have the nanostructure", has been amended as described above, and now recites an electrically insulating spacer structure that coats the via hole. The spacer structure is shown in Fig. 2 (reference numeral 201) of the drawings. Thus, it is believed that the drawings comply with 37 CFR 1.83(a).

In the Specification

The Examiner objected the title because the title of the invention is not descriptive. Applicants have amended the title. Applicants believe the title is now in condition for allowance.

The Examiner objected to the disclosure because it contains an embedded hyperlink and/or other form of browser-executable code. Applicants have amended the specification to correct this informality. Applicants believe the Specification is now in condition for allowance.

The Examiner objected to the disclosure because it contains an informality. Conductive Layer 103 has been deleted and conductive layer 105 has been inserted. Applicants have amended the specification to correct this informality. Applicants believe the Specification is now in condition for allowance.

Claim Rejections under 35 U.S.C. § 102

The Examiner rejected claims 22-25, 33-36, and 38-43 under 35 U.S.C. § 102(b) as being anticipated by the Mancevski et al. U.S. Publication No. 2001/0023986.

Applicant has amended claim 22 to include features from claim 26, which is now canceled. Amended claim 22 recites a vertically integrated field-effect transistor including, a first electrically conductive layer, a middle layer, formed partially from dielectric material, on the first electrically conductive layer, a second electrically conductive layer on the middle layer, and a nanostructure integrated in a via hole introduced into the middle layer. The nanostructure includes a first end portion that is coupled to the first electrically conductive layer and a second end portion that is coupled to the second electrically conductive layer. The first end portion of the nanostructure forms a first source/drain region and the second end portion of the nanostructure forms a second source/drain region of the field-effect transistor. The middle layer, between two adjacent dielectric sublayers, has a third electrically conductive layer, the thickness of which is less than the thickness of at least one of the dielectric sublayers. ***A ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein***.

As the Examiner has agreed, the Mancevski reference fails to teach or suggest a ring structure as gate-insulating region of a field-effect transistor having a nanostructure integrated in a via hole. Thus, the subject-matter of claims 22 and its dependant claims 23-25 allowable over the art of record. Similarly, claims 41 and 43 have been similarly amended to include similar features that are not taught or suggested by the Mancevski reference. As such, the subject-matter of claims 41-43 are allowable over Mancevski for at least the same reasons.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 102(b) rejection to claims 22-25, 33-36, and 38-43, and request allowance of these claims.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 26-28, 30-32, and 37 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Publication No. 2001/0023986.

As indicated above, claim 22 as amended, now recites a vertically integrated field-effect transistor including a nanostructure integrated in a via hole, and further including a first, second and third electrically conductive layer, wherein a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in the third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that has been introduced therein.

The Mancevski reference discloses a carbon nanotube transistor that includes a carbon nanotube having two or more defects, wherein the defects divide the carbon nanotube into three regions having different conductivities (see e.g. Abstract and paragraph [0021] in Mancevski). With respect to Figure 2 (also compare paragraph [0040]), Mancevski discloses vertical carbon nanotube transistor devices, each of the transistors including a vertically aligned carbon nanotube 14a, 14b, 14c, 14d that is grown from a first contact plane 16. The nanotubes are grown within vertically aligned holes within a substrate material. A second contact plane 20 is provided allowing conductive interconnects 22a, 22b, and 22c to contact gates 24a, 24b, 24c, and 24d of the transistors. An upper portion of each nanotube is electrically connected in a third contact plane 28.

Each nanotube has two defects that divide the nanotube into three different regions 36, 38, and 40 along the length of the nanotube, the three regions having different conductivities. As can be inferred from the caption of Figure 2, regions 36 and 40 correspond to conductive regions of the carbon nanotube, whereas region 38 is a semiconductive region of the carbon nanotube.

The Mancevski reference neither discloses nor suggests that an electrically insulating structure is formed as gate-insulating region in one or more of the vertically aligned holes in order to electrically insulate the carbon nanotubes 14a, 14b, 14c, and 14d from the gates 24a, 24b, 24c, and 24d. In particular, Mancevski neither discloses nor suggests an electrically insulating ring structure as gate insulator.

Figure 2 of the Mancevski reference shows that the gates 24a, 24b, 24c, and 24d correspond to semiconductive segments of the respective carbon nanotubes 14a, 14b, 14c, and 14d (cf. caption of Figure 2), and that the gates are electrically contacted by the conductive interconnects 22a, 22b, and 22c. In other words, as the gates 24a, 24b, 24c, and 24d are segments of the nanotubes 14a, 14b, 14c, and 14d, the nanotubes themselves are electrically contacted by the interconnects 22a, 22b, and 22c. However, no gate-insulting region of whatever shape or structure is discloses or suggested by the Mancevski reference or the art of record.

Futhermore, Figure 3 in the Mancevski reference, which illustrates steps of a process for fabricating the carbon nanotube transistor devices, shows that in a carbon nanotube 56 having upper and lower segments of a first diameter (which correspond to conductive segments of the nanotube), and a middle segment of a second diameter greater than the first diameter (which corresponds to a semiconductive segment of the nanotube), each of the three segments is electrically contacted by means of respective electrical contacts 57a, 57b, and 57c. Again, no electrically insulating structure or region is shown or suggested.

The Mancevski reference discloses a vertical carbon nanotube transistor based on a vertically aligned carbon nanotube having three regions or segments of different conductivities (namely two conductive segments and one semiconductive segment in-between), each of the three regions being electrically contacted. However, the Mancevski reference neither discloses nor suggests a vertically integrated field effect transistor in accordance with amended claim 22, wherein first and second portions of a nanostructure are coupled to first and second electrically conductive layers, respectively, and wherein a ring structure formed from an electrically insulating material as gate-insulating region of the field-effect transistor is arranged in a third electrically conductive layer, which forms the gate electrode of the field-effect transistor, along the via hole that ha been introduced.

One effect of the ring structure as gate insulting region is that on account of the ring-like structure of the gate-insulting layer, an electric field which is generated on account of an electrical potential applied to the third electrically conductive layer may act sufficiently well over the nanostructure, which is attributable to the gate electrode, which is electrically insulated

by means of the gate-insulating layer, surrounding the nanostructure on all sides.

Because the Mancevski reference neither discloses nor suggests the subject-matter of amended claim 22, the subject-matter of amended claim 22 is believed to allowable over the Mancevski reference. Claims 41 and 43, which have been amended in a similar manner, are allowable for the same reasons, as are dependant claim 23-25, 27-40, and 42. Thus, the subject-matter of claims 23-25 and 27-42 is believed to be non-obvious over Mancevski for at least the same reasons.

The Examiner rejected claim 29 under 35 U.S.C. § 103(a) as being unpatentable over the Mancevski U.S. Publication No. 2001/0023986 in view of the Martin et al. U.S. Publication No. 2001/0019279.

Because claim 29 is dependant on an allowable claim as discussed above, it too is in proper form for allowance. Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 103 rejection to claims 26-32, and 37, and request allowance of these claims.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 22-25 and 27-43 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 22-25 and 27-43 are respectfully requested.

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Paul P. Kempf at Telephone No. (612) 767-2502, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

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